REMARKS

Claims 1-20 remain in the present application. Claims 1, 10 and 17 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the arguments set forth below.

Claim Rejections – 35 U.S.C. §112

Claims 1-16 are rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. Applicants respectfully submit that Claims 1-16, based upon the amendments to independent Claims 1 and 10, comply with 35 U.S.C. 112, first paragraph.

Claim Rejections – 35 U.S.C. §103

Claims 1-3, 6, 10-11 and 15-16

Claims 1-3, 6, 10-11 and 15-16 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over United States Patent Number 5,994,937 to Hara et al. (hereafter referred to as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (hereafter referred to as "Kwon"), and further in view of United States Patent Number 6,031,366 to Mitsuishi (hereafter referred to as "Mitsuishi"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 6, 10-11 and 15-16 are not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising (emphasis added):

an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and

a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, wherein said plurality of selectively-activated components comprise components different from components of said circuit for providing a selectable amount of pull down current, said pull-down path also coupled to receive a reference signal that varies in proportion to temperature, and wherein said delay through said timer circuit is inversely proportional to said temperature.

Independent Claim 10 recites similar limitations to independent Claim 1. Claims 2-3, 6, 11 and 15-16 depend from their respective independent claims and recite further limitations to the claimed invention.

Applicants respectfully submit that Hara fails to teach or suggest the limitation of "wherein said plurality of selectively-activated components comprise components different from components of said circuit for providing a selectable amount of pull down current" as recited in independent Claim 1. As recited and described in the present application, a configurable delay element coupled to an output stage comprises a plurality of selectively-activated components. Additionally, a pull-down path coupled to the output stage comprises a circuit for providing a selectable amount of pull down current. The plurality of selectively-activated components comprise components *different from* components of the circuit for providing a selectable amount of pull down current.

In contrast to the claimed embodiments, Applicants understand Hara to teach a circuit with identical components. For example, Figure 4 of Hara shows circuit 400 with N-FET 414 and N-FET 424, which are understood by Applicants to be identical components since both are N-FETs. As such, assuming arguendo that N-FET 424 is analogous to a circuit for providing a selectable amount of pull down current as claimed (as suggested by page 3 of the

rejection), and also assuming arguendo that N-FET 414 is analogous to a configurable delay element as claimed (as suggested by page 4 of the rejection), Applicants respectfully submit that Hara teaches away from the claimed embodiments by teaching *identical* components instead of *different* components as claimed.

Applicants respectfully submit that both Kwon and/or Mitsuishi, either alone or in combination with Hara and/or one another, fail to cure the deficiencies of Hara discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Kwon and Mitsuishi also fail to teach or suggest the limitation of "wherein said plurality of selectively-activated components comprise components different from components of said circuit for providing a selectable amount of pull down current" as recited in independent Claim 1.

Applicants respectfully submit that Hara, Kwon and/or Mitsuishi, either alone or in combination with one another, fail to teach or suggest the limitations of "a first transistor having a gate controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal" as recited in independent Claim 6. As recited and described in the present application, the circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel. Each gated pull-down circuit comprises a first transistor having a gate controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by the reference signal (e.g., which varies with temperature).

In contrast to the claimed embodiments, Applicants understand Hara as modified by Mitsuishi's Figure 3 to teach a transistor which is coupled to a bias voltage (VB) and which functions as a constant current source (col. 4, lines 44-45). Since the transistor (e.g., M_1 to M_n as shown in Figure 3 of Mitsuishi) functions as a *constant* current source, then Applicants respectfully submit that VB is also constant and does not vary. As such, assuming arguendo that a transistor (e.g., M_1 to M_n) as taught by Mitsuishi is analogous to a second transistor coupled to a reference signal as claimed, Applicants respectfully submit that Mitsuishi teaches away from the claimed embodiments by teaching a transistor coupled to a constant VB instead of a transistor coupled to a reference signal which varies with temperature as claimed.

For these reasons, Applicants respectfully submit that independent Claim 1 is not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since independent Claim 10 recites limitations similar to those discussed above with respect to independent Claim 1, independent Claim 10 also overcomes the 35 U.S.C. §103(a) rejections of record. Since Claims 2-3, 6, 11 and 15-16 recite further limitations to the invention claimed in their respective independent claims, Claims 2-3, 6, 11 and 15-16 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-3, 6, 10-11 and 15-16 are allowable.

Claims 1-16

Claims 1-16 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of United States Patent Number 6,388,490 to Saeki (hereafter referred to as "Saeki"). Applicants have reviewed the cited references and respectfully

submit that the embodiments of the present invention as recited in Claims 1-16 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine Saeki, in the claimed fashion, with the cited Hara/Kwon/Mitsuishi combination. For example, pages 3-4 of the rejection suggest replacing Hara's N-FET 424 with Mitsuishi's Figure 3 to create a circuit for providing a selectable amount of pull-down current as claimed, and pages 3-4 of the rejection also suggest replacing N-FET 414 with Mitsuishi's Figure 3 to create a configurable delay element as claimed. As discussed above, Hara teaches that elements 414 and 424 are identical (e.g., both N-FETs). Additionally, the rejection suggests that Hara's elements 414 and 424, as modified, are also identical since each of the N-FETs are replaced by the same circuit (e.g., Mitsuishi's Figure 3). Further, page 3 of the rejection states that both elements (e.g., 414 and 424) are identical "in order to ensure a balance [sic] output signal." Accordingly, to reiterate, the cited Hara/Kwon/Mitsuishi combination teaches identical components (e.g., Hara's elements 414 and 424), thereby teaching away from the claimed embodiments as discussed above.

However, page 5 of the rejection suggests that it would be obvious to one of ordinary skill in the art to replace Hara's N-FET 414 with Saeki's capacitors (e.g., CAP11-CAP15 as shown in Figure 3 of Saeki). Applicants respectfully submit that such a modification would render Hara's circuit with non-identical elements 414 and 424. Accordingly, both the cited Hara/Kwon/Mitsuishi combination as well as page 3 of the rejection teach away from such a combination since both the cited Hara/Kwon/Mitsuishi combination and page 3 of

the rejection teach/state that elements 414 and 424 should be identical. Thus, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine Saeki with the cited Hara/Kwon/Mitsuishi combination in the claimed fashion.

For these reasons, Applicants respectfully submit that independent Claims 1 and 10 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since Claims 2-9 and 11-16 recite further limitations to the invention claimed in their respective independent claims, Claims 2-9 and 11-16 also overcome the 35 U.S.C. §103(a) rejection of record. Therefore, Claims 1-16 are allowable.

Claims 17-20

Claims 17-20 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 17-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;
> during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down

path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and

during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying of said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further limitations to the claimed invention.

Applicants respectfully submit that Hara, Kwon and/or Mitsuishi, either alone or in combination, fail to teach or suggest the limitations of "during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit," "during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage," and "during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying of said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit" as recited in independent Claim 17. As recited and described in the present application, a timer circuit may be placed in a configuration mode and an operation mode. While in the configuration mode, configuration bits are set to control the delay through the timer circuit by determining an amount of elements coupled to the output stage of the timer circuit. Additionally, while in the configuration mode, a second set of configuration bits are set during configuration to control an amount of pull-down current of the timer circuit. Further, when placed in the operation mode, the delay of the timer circuit is varied inversely proportional to a temperature of the timer circuit.

In contrast to the claimed embodiments, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest a plurality of distinguishable modes as claimed. Additionally, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest such a plurality of distinguishable modes comprising a configuration mode and an operation mode as claimed. Further, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest setting a plurality of configuration bits to control pull down current *during configuration* (as opposed to during operation) as claimed. For example, even if Mitsuishi's switches and transistors as depicted in Figure 3 of Mitsuishi were added to Hara's circuit depicted in Figure 4 of Hara, neither reference teaches or suggests that adjustment of the switches are performed *during a configuration mode* as claimed. Accordingly, Applicants reiterate that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest the limitations of "during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit," "during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage," and "during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said varying of said delay of said timer circuit comprises varying said delay inversely proportional to a temperature of said timer circuit" as recited in independent Claim 17.

Furthermore, page 7 of the rejection states that "the configuration period may be any period, and the operation period may be any period different from the configuration period." Applicant wishes to respectfully remind the Examiner that "the examiner should set forth in the Office action: (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate" and "(B) the difference or differences in the claim over the applied reference(s)" (MPEP §706.02(j)). As such, a mere assertion that distinguishable configuration and operation periods may exist does not provide Applicants sufficient guidance as to the relevant teachings of the prior art relied upon as required by the MPEP (e.g., with column and line number references), nor does it set forth the difference or differences in the claim over the applied references. Therefore, Applicants respectfully request appropriate correction to the rejection pertaining to Claim 17 in the next Office Action if the rejection is to be maintained.

For these reasons, Applicants respectfully submit that independent Claim 17 is not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since Claims 18-20 recite further limitations to the invention claimed in independent Claim 17, Claims 18-20 also overcome the 35 U.S.C. §103(a) rejection of record. Therefore, Claims 17-20 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 2/22, 2008

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